Q1) Using standard paging scheme, map the following logical addresses to their respective physical addresses. Page size is 4 bytes and physical memory is 32 bytes.

A picture containing text, device, thermometer, screenshot

Description automatically generated

* Logical address is <page# 2, offset 2> :
* Logical address <page#4, offset 0>:

Q2) Consider the following segment table. For each logical address, determine the physical address if any.

* 0, 320
* 1.20
* 2,490
* 3,400

|  |  |  |
| --- | --- | --- |
| **Segment** | **Base** | **Length** |
| 0 | 219 | 600 |
| 1 | 2300 | 14 |
| 2 | 90 | 100 |
| 3 | 1327 | 580 |

Q3) Assume the page size is 1024 bytes and the process size is 2100 bytes. Calculate the internal fragmentation, if any.

Q4) Consider that PT is stored in physical memory, the memory access time is 100ns and the access time to associative memory is 10ns. If the hit ratio is 80%, calculate EAT?

Q5) Consider a logical address space of 256 pages with a 2-KB page size, mapped onto a physical memory of 32 frames. How many bits are required in the logical address and in the physical address?

Q6) Consider a 64-bit logical address space, page size of 4 KB.

* How many entries will be in the PT?
* If each entry in PT is 4 bytes, what is the size of the PT in bytes?